REMARKS

Summary of the Response

Upon entry of the present amendment, claim 1 will be amended, whereby claims 1, 2 and 4 remain pending with claim 1 being the sole independent claim.

While not expressing agreement with or acquiescence to the rejections of record, claim 1 has been amended to even more clearly recite the vias including that the "vias are made in via holes the insulating layer which electrically and directly connect the semiconductor-surface-electrodes and the mount-surface-electrodes." Support for the amendment to claim 1 appears in Applicants' originally filed application, including Figures 1, 2 and 9. Accordingly, no new mater has been introduced by the present amendment.

Reconsideration of the rejections of record and allowance of the application in view of the following remarks are respectfully requested.

Summary of the Office Action

In the instant Office Action, the Examiner has rejected claims 1, 2 and 4 over the art of record. By the present remarks, Applicants submit that the rejections have been overcome, and respectfully request reconsideration of the outstanding Office Action and allowance of the present application.

Traversal of Rejection Under 35 U.S.C. § 103(a)

The examiner bears the initial burden of factually supporting any *prima facie* conclusion of obviousness. If the examiner does not establish a *prima facie* case, the applicant is under no obligation to submit evidence of nonobviousness. See MPEP §2142. To establish a *prima facie*

case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the art or to combine reference teachings.[1] Second, there must be a reasonable expectation of success. Finally, the document (or documents when combined) must teach or suggest all the claim limitations. The teaching or suggestion to make the claimed combination and the reasonable expectation of success must both be found in the prior art, and not based on applicant's disclosure. *In re Vaeck*, 947 F.2d 488, 20 USPQ2d 1438 (Fed. Cir. 1991).

1. *Over INOUE in view of CHEN and OOHATA*

Applicants respectfully traverse the rejection of claims 1 and 2 under 35 U.S.C. § 103(a) as being unpatentable over U.S. Patent No. 6,333,522 to Inoue et al. (hereinafter INOUE) in view of U.S. Patent Publication No. 2004/0026708 to Chen (hereinafter CHEN) and U.S. Patent Publication No. 2003/0160258 to Oohata (hereinafter OOHATA).

Independent Claim 1

The present invention is directed to a light-emitting device. Claim 1 recites, in pertinent part:

> . . . an insulating layer which holds the semiconductor layers, said insulating layer comprising two surfaces; and
>
> mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder, the

[1] While the *KSR* court rejected a rigid application of the teaching, suggestion, or motivation ("TSM") test in an obviousness inquiry, the [Supreme] Court acknowledged the importance of identifying "a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does" in an obviousness determination. *Takeda Chemical Industries, Ltd. v. Alphapharm Pty., Ltd.*, 492 F.3d 1350, 1356-1357 (Fed. Cir. 2007) (quoting *KSR International Co. v. Teleflex Inc.*, 127 S.Ct. 1727, 1731 (2007)).

> mount-surface-electrodes being provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made;
>
> wherein one of the semiconductor layers has a non-deposited area where the other semiconductor layer is not deposited;
>
> one of the semiconductor-surface-electrodes is built up on the surface of the non-deposited area;
>
> vias are made in via holes in the insulating layer which electrically and directly connect the semiconductor-surface-electrodes and the mount-surface-electrodes, the via holes are filled with solder or electric conductive paste;
>
> the semiconductor-surface-electrodes, the insulating layer, and the mount-surface-electrodes are built up in this order on one side of the deposited semiconductor layers; and
>
> a surface of the other side of the deposited semiconductor layers is a light emitting surface which emits light beams directly to outside from the semiconductor layers.

Applicants submit that the combination of documents does not teach or suggest each of the features of the present invention. For example, Applicants submit the combination of references at least do not teach or suggest: (1) the mount-surface-electrodes being provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made; (2) vias are made in via holes in the insulating layer which electrically and directly connect the semiconductor-surface-electrodes and the mount-surface-electrodes; (3) via holes are filled with solder or electric conductive paste; and (4) an insulating layer which holds the semiconductor layers.

Additionally, Applicants submit that the references teach away from the Examiner-proposed modifications (i.e., including mount-surface-electrodes structured and arranged to mount the light-emitting device onto a mounting substrate by using solder, as purportedly taught by CHEN; and removing the sapphire layer of INOUE). Furthermore, Applicants submit the rejection is *per se* improper, as the Examiner has designated the same element of INOUE as two distinct features of the present invention.

The insulating layer of present application is a insulating layer holding the semiconductor layers, and therefore the semiconductor layers can be held only by the insulating layer. This insulating layer has mount surface electrodes on its surface which are structured and arranged to mount the light-emitting device onto a mounting substrate by using solder. As shown in the figures of present application, the insulating layer in the invention of present application having the above-mentioned function has sufficient strength and thickness to maintain the form of the semiconductor layers steady while holding the semiconductor layers, and also has a outer shape same as the outer shape of the semiconductor layers to hold uniformly the entire semiconductor layers. Additionally, the surface of the insulating layer is made flat to structure and arrange the mount-surface-electrodes. Thus, the insulating layer in the invention of present application is not only a passivation layer but a layer to hold the semiconductor layers.

When a light-emitting device in accordance with the present invention is mounted onto a mounting substrate, the semiconductor layers of the light-emitting device are connected by solder and mount-surface-electrodes to the substrate. The light emitting device provided with such mount-surface-electrodes can be mounted on a substrate by using surface mount technologies.

No Teaching Or Suggestion Of Mount-Surface-Electrodes Provided On One Surface Of The Insulating Layer Which Is Opposite To The Other Surface Of The Insulating Layer Where The Semiconductor-Surface-Electrodes Are Made

In addressing previously presented claim 1, the Examiner designates the microbumps 24 and 25a of INOUE as the recited mount surface electrodes and designates the passivation layer 29 of INOUE as the recited insulation layer. Moreover, the Examiner asserts INOUE teaches "the mount-surface-electrodes 25a, 24 provided on one surface of the insulating layer which is

opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes 5, 6 are made." Applicants respectfully disagree.

Applicants submit that the Examiner-designated mount surface electrodes (i.e., microbumps 24 and 25a) are not provided on one surface of the Examiner-designated insulating layer, which is opposite to the other surface of the Examiner-designated insulating layer where the semiconductor-surface electrodes are made. That is, even if the microbumps 24 and 25a can reasonably be construed as mount surface electrodes and the passivation layer 29 can reasonably be construed as the recited insulating layer (neither of which Applicants concede), as shown in Figure 7B of INOUE, the microbumps 24 and 25a are not formed on a surface of the Examiner-designated insulating layer opposite to the other surface of the Examiner-designated insulating layer where the semiconductor-surface electrodes are made.

Applicants submit the microbumps 24, 25a of INOUE are solid construction electrodes formed by penetrating the passivation layer 39 from semiconductor surface electrodes 5, 6 at the semiconductor layers 31-35 and protruding from the surface of the passivation layer 39. The top of the integrated shape of such micro-bump is used to mount the light emitting device.

As clearly illustrated in Figure 7B, however, no part of the Examiner-designated mount surface electrodes are formed on a surface of the Examiner-designated insulating layer opposite to the other surface of the Examiner-designated insulating layer where the semiconductor-surface electrodes are made. That is, Applicants submit the microbumps 24 and 25a do not contact an upper surface of the passivation layer 29. As such, for at least these reasons, Applicants submit INOUE does not teach or suggest the mount-surface-electrodes being provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made, as recited in claim 1.

No Teaching or Suggestion of Vias Made In The Insulating Layer Which Electrically And Directly Connect The Semiconductor-Surface-Electrodes And The Mount-Surface-Electrodes

In addressing previously presented claim 1, the Examiner designated the holes formed in the insulating layer 39 as via holes which electrically connect the Examiner-designated semiconductor-surface-electrodes (i.e., microbumps 24 and 25a) and the Examiner-designated mount-surface-electrodes (i.e., electrodes 5 and 6). Applicants respectfully disagree.

Applicants respectfully submit that the Examiner-designated via holes do not electrically connect the Examiner-designated semiconductor-surface-electrodes (i.e., microbumps 24 and 25a) and the Examiner-designated mount-surface-electrodes (i.e., electrodes 5 and 6). That is, the Examiner-designated via holes constitute an absence of material (i.e., passivation material of layer 39). As such, the Examiner-designated via holes themselves cannot electrically connect the Examiner-designated semiconductor-surface-electrodes (i.e., microbumps 24 and 25a) and the Examiner-designated mount-surface-electrodes (i.e., electrodes 5 and 6), as the Examiner asserts.

In contrast to INOUE, with the present invention, vias are made in the insulating layer which electrically and directly connect the semiconductor-surface-electrodes and the mount-surface-electrodes. For example, the vias may comprise an electrical conductor 51 provided on the inner wall of the via holes 41. See, e.g., paragraph [0078] of the present application (as numbered in published application No. 2006/0231853.

Thus, for at least these reasons, Applicants submit INOUE does not teach or suggest vias are made in the insulating layer which electrically and directly connect the semiconductor-surface-electrodes and the mount-surface-electrodes, as recited in claim 1.

No Teaching or Suggestion of Via Holes Filled With Solder Or Electric Conductive Paste

The electric conductive paste used to fill via holes in present application, is made by mixing heat-hardening resin or solvent medium with, for example, electric conductive particles of Cu, Ag, Al etc. as-is or those particles having coating made of low melting point metal. The electric conductive paste comprises many electric conductive particles that are electrically and thermally in contact each other.

In addressing previously presented claim 1, the Examiner asserts INOUE teaches via holes are filed with solder or electric conductive paste, referring to column 26, lines 52 - 56, which discuss the material of the microbumps 25a and 24. Additionally, in the Response to Arguments, the Examiner states:

> [T]he via holes are the holes that are formed in the insulating layer 39 wherein conductive elements 25a, 24 are form [sic] (or filled in) as shown in figure 7B, and since conductive elements 25a, 24 (micro-bumps) are made of Au (electric conductive paste) and filled in the via holes, it can be considered that the via holes are filled with electric conductive paste. It is noted that there is no specific material recited for the claimed electric conductive paste such that Au, which is electric conductive material, can be construed as "electric conductive paste" herein. In other words, [INOUE] discloses the via holes are filled with electric conductive paste.

Initially, Applicants submit that the Examiner is improperly designating the microbumps 25a and 24 as both the recited mount-surface-electrodes and as the recited solder or electric conductive paste. As such, Applicants submit the rejection is *per se* improper. That is, while the Examiner is entitled to make alternative rejections, in rejecting a claim the Examiner is not permitted to designate the same element of the prior art as multiple distinct elements of the claimed invention.

Additionally, even if the Examiner's designation of the microbumps 25A and 24 as the recited solder or electric conductive paste is proper, Applicants submit INOUE does not teach or

suggest via holes are filed with solder or electric conductive paste. Applicants note the Examiner cited passage merely states

> The material of the micro-bumps may be a solder material or an Au-based material. Although either of the solder material and the Au-based material may be used as the material of the micro-bumps according to the present invention, the Au-based material is preferable to the solder material.

In contrast to the Examiner's assertions, Applicants submit INOUE teaches, at column 26, line 62 - column 27, line 37, that the microbumps 25a and 24 are formed by plating a stud bump method or a plating method. That is, the microbump material (i.e., Au) is deposited by electroplating, or a chip of Au wire is cut during stud-bump forming. As is understood by those ordinarily skilled in the art, the micro-bump formed using the stud bump method or a plating method provides for a uniform inner structure to the microbump. However, as described in INOUE, neither of these microbump forming processes utilize an electric conductive paste. Moreover, as would be understood by an ordinarily skilled artisan, a via made of electric conductive paste lacks a uniform inner structure, in contrast to the microbump of INOUE having the uniform inner structure.

Moreover, Applicants note that INOUE is completely silent with respect to an "electric conductive paste." As such, Applicants submit the Examiner is merely asserting that an Au layer is an electric conductive paste without providing any support in the cited document for such an assertion.

Thus, for at least these reasons, Applicants submit INOUE fails to teach or suggest via holes are filled with solder or electric conductive paste, as recited in claim 1.

No Teaching or Suggestion of An Insulating Layer Which Holds The Semiconductor Layers

In addressing previously presented claim 1, the Examiner asserts INOUE teaches an insulating layer that holds the semiconductor layers. Applicants submit, however, that the Examiner-designated insulating layer (i.e., passivation layer 39) does not hold the Examiner-designated semiconductor layers (i.e., layers 32 and 35), and that one of ordinary skill in the art would not consider the passivation layer 39 to be holding the Examiner-designated semiconductor layers (i.e., layers 32 and 35). Instead, Applicants submit the sapphire substrate of INOUE holds the semiconductor layers (e.g., layers 31 - 35). Moreover, if the sapphire substrate were to be removed (as the Examiner proposes in the rejection of claim 1, which is discussed further below), there is no teaching or suggestion that the passivation layer is operable to hold the semiconductor layers in form as a light emitting diode.

As such, for at least these reasons, Applicants submit INOUE fails to teach or suggest an insulating layer which holds the semiconductor layers, as recited in claim 1.

Moreover, Applicants submit that neither CHEN nor OOHATA compensates for the above-noted deficiencies of INOUE (i.e., (1) the mount-surface-electrodes being provided on one surface of the insulating layer which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made; (2) vias are made in via holes in the insulating layer which electrically and directly connect the semiconductor-surface-electrodes and the mount-surface-electrodes; (3) via holes are filled with solder or electric conductive paste; (4) an insulating layer which holds the semiconductor layers). For example, the welding metals 41 of CHEN are electrodes formed on the electrodes 20, 22 on the semiconductor layer are not formed on the insulating layer surface (i.e., layer 42), as recited in claim 1. Furthermore, Applicants

note the Examiner did not assert that CHEN or OOHATA teach or suggest the above-discussed features of the present invention, and only relied upon these documents for their purported teachings of additional features of the present invention (which are discussed below). As such, no reasonable combination of these documents renders unpatentable the presently claimed invention.

CHEN Teaches Away From Mount-Surface-Electrodes Being Structured And Arranged To Mount The Light-Emitting Device Onto A Mounting Substrate By Using Solder

In addressing previously presented claim 1, the Examiner acknowledges that INOUE fails to teach or suggest mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder. However, the Examiner asserts CHEN teaches mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder, and that it would have been obvious to modify INOUE to include mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder so as to improve the inject current capability in a light emitting device. Specifically, the Examiner asserts "in paragraph [0009] Chen teaches of a welding metal 41, which can function as 'mount surface electrodes' herein" and asserts that the welding metal 41 of CHEN corresponds with the mount-surface-electrodes of present application. Additionally, the Examiner asserts that it would have been obvious to modify INOUE in view of CHEN "so as to improve the inject current capability in a light emitting device. Applicants respectfully disagree.

Applicants respectfully submit that CHEN teaches away from the Examiner-proposed modification. Applicants note that a prior art reference must be considered in its entirety, i.e., as

a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). While acknowledging CHEN does discuss welding material 41 in paragraph [0009], Applicants note that this discussion is of the prior art (and its deficiencies) that CHEN is expressly directed to overcoming. For example, CHEN states at paragraph [0010] that (emphasis added):

> In the example mentioned foregoing, Wierer et al proposed the technique for a LED chip mounting on the silicon submount so that the inject current capability is improved, but there are room for further improvement. For example, the thermal conductivity of silicon submount is not as good as some high thermal conductivity metal such as aluminum and copper. Besides, the thermal conductivity of silicon is getting worse as the temperature increasing. Therefore, the object of the invention is thus to propose a new package techniques by means of using the metal substrate as the submount to solve aforementioned problem.

Applicants submit that CHEN specifically teaches that the mounting approach (i.e., using welding metal 41) utilized in the discussed prior art is deficient, and thus, is directed to improving this mounting approach. As such, Applicants respectfully submit that CHEN teaches away from the Examiner-proposed modification. Thus, Applicants submit that one of ordinary skill in the art would not be motivated to modify INOUE in view of CHEN in a manner from which CHEN specifically teaches away. Accordingly, Applicants submit the combination of INOUE and CHEN does not teach or suggest mount-surface-electrodes being structured and arranged to mount the light-emitting device onto a mounting substrate by using solder.

INOUE Teaches Away From Examiner-Proposed Modification

In addressing claim 1, the Examiner acknowledges that INOUE fails to teach or suggest a light emitting surface that emits light beams directly to outside. However, the Examiner asserts

OOHATA discloses a light emitting surface that emits light beams directly to outside, and that it would be obvious to one of ordinary skill in the art to modify INOUE in view of OOHATA by removing the sapphire layer of INOUE. Applicants respectfully disagree.

Initially, Applicants submit OOHATA fails to disclose a light emitting surface that emits light beams directly to outside, as the Examiner asserts. Applicants submit the light emitting diode device in figure 1 of OOHATA has a semiconductor surface electrode 5 on the surface of the semiconductor layers (1,2,3) which surface emits light beams (arrow) to outside. That is to say, the light emitting diode device of OOHATA is a device having semiconductor surface electrodes 5, 9 on both surfaces of the semiconductor layers (1,2,3), and not a device of structure of the invention according to present claim 1 that "the semiconductor-surface-electrodes, the insulating layer, and the mount-surface-electrodes are built up in this order on one side of the deposited semiconductor layers." Applicants note that the light emitting diode device in Figure 1 of OOHATA employs cathode take-out electrode 6 to connect cathode contact electrode 5 on one side of the semiconductor layers and lead-out electrode 8 on the other side of the semiconductor layers through via 7 (see paragraph [0056]). Moreover, this light emitting diode device of OOHATA, at the portion of semiconductor surface electrodes 5, is not a device comprising semiconductor layers (1,2,3) which emits light beams (arrow) directly to outside. The light emitting diode device in figure 1 of OOHATA is a device having a different structure from the device structure of present application, and also includes semiconductor surface electrodes 5 which interferes with semiconductor layers emitting light beams (arrow) directly to outside. As such, Applicants submit OOHATA fails to teach or suggest a light emitting diode device having "a surface of the other side of the deposited semiconductor layers is a directly light emitting surface."

Furthermore, Applicants submit INOUE teaches away from the Examiner-proposed modification. That is, modifying INOUE as the Examiner asserts would render INOUE unsuitable for its intended purpose. Applicants note that a prior art reference must be considered in its entirety, i.e., as a whole, including portions that would lead away from the claimed invention. *W.L. Gore & Associates, Inc. v. Garlock, Inc.*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), *cert. denied*, 469 U.S. 851 (1984). Applicants note that if a proposed modification would render the prior art invention being modified unsatisfactory for its intended purpose, then there is no suggestion or motivation to make the proposed modification. *In re Gordon*, 733 F.2d 900, 221 USPQ 1125 (Fed. Cir. 1984). Additionally, Applicants note that if the proposed modification or combination of the prior art would change the principle of operation of the prior art invention being modified, then the teachings of the references are not sufficient to render the claims *prima facie* obvious. *In re Ratti*, 270 F.2d 810, 123 USPQ 349 (CCPA 1959).

Applicants submit modifying INOUE in view of CHEN and OOHATA in the manner asserted by the Examiner (i.e., by removing the sapphire substrate) would render INOUE unsatisfactory for its intended purpose. INOUE states at column 1, lines 12 - 16 that (emphasis added), "[i]n particular, the present invention is properly applicable to a light-emitting element (LED) using a gallium-nitride-based compound semiconductor formed on a sapphire substrate and to a light-emitting device comprising such a light-emitting element.

Additionally, INOUE states at column 11, line 66 - column 12, line 15 that (emphasis added):

> The substrate may be made of a material transparent under the light emitted from the light-emitting element. This permits the light emitted from within the element to be obtained from the substrate side and efficient emission of light with a flip-chip structure. In the case where the light-emitting element is made of a GaN-based compound semiconductor, the substrate is preferably made of sapphire. Since an excellent

> crystallographic compatibility is observed between a GaN crystal and a sapphire crystal and the sapphire substrate is a transparent insulating substrate, the resulting flip-chip light-emitting element is excellent in the property of emitting light including blue light. The sapphire substrate [i]s also superior and convenient in terms of light-emitting efficiency since the refractive index of the sapphire substrate, which is 1.77, is between the refractive index of GaN, which is 2.1, and the refractive index of a mold resin, which is 1.5.

Furthermore, INOUE states at column 24, lines 54 - 63 that (emphasis added):

> [b]ecause the sapphire substrate 30 is high in melting point, the present embodiment has the advantage of forming a silicon single-crystal thin film extremely easily by a laser recrystallization method after the deposition of a polysilicon film. Moreover, since the present embodiment can easily be constituted such that light is emitted from the underlying sapphire substrate, it is possible to maintain high light-emitting efficiency even when the GaN LED element 1 is connected to the diode element 60 by wire bonding.

Applicants submit that INOUE is directed to a light-emitting element formed on a substrate, and more particularly, formed on a sapphire substrate. Moreover, Applicants submit that the sapphire substrate of INOUE provides the advantageous relative refractive index and high melting point, as noted in the above-cited portions.

As such, Applicants submit modifying INOUE in view of CHEN and OOHATA in the manner asserted by the Examiner (i.e., by removing the sapphire substrate) would render INOUE unsatisfactory for its intended purpose of providing the advantageous relative refractive index and high melting point. That is, by removing the sapphire substrate layer of INOUE, the light-emitting element of INOUE would no longer include the transparent substrate, let alone a sapphire substrate.

Thus, Applicants submit INOUE teaches away from the Examiner-proposed modification, in that the Examiner-proposed modification would render INOUE unsatisfactory

for its intended purpose. Thus, Applicants submit there is no suggestion or motivation to make the proposed modification, and the Examiner has failed to set for a *prima facie* case of obviousness.

Thus, for these additional reasons, Applicants submit no reasonable combination of these documents renders unpatentable the presently claimed invention. Accordingly, for at least the above-discussed reasons, Applicants request the Examiner withdraw the rejection of claim 1, and indicate claim 1 as allowable.

Dependent Claim 2

With regard to claim 2, Applicants respectfully submit claim 2 depends from distinguishable independent claim 1, and is allowable based upon the allowability of independent claim 1, and because this claim recites additional subject matter to further define the instant invention.

Accordingly, for at least these reasons, Applicants request the Examiner withdraw the rejection of claims 1 and 2, and indicate claims 1 and 2 as allowable.

2. Over *INOUE in view of CHEN, OOHATA and LOWERY*

Applicants respectfully traverse the rejection of claim 4 under 35 U.S.C. § 103(a) as being unpatentable over INOUE in view of CHEN and OOHATA, and further in view of U.S. Patent No. 6,878,973 to Lowery et al. [hereinafter LOWERY].

Applicants submit LOWERY does not cure the above-noted deficiencies of INOUE in view of CHEN and OOHATA. For example, Applicants submit LOWERY fails to teach or suggest: (1) the mount-surface-electrodes being provided on one surface of the insulating layer

which is opposite to the other surface of the insulating layer where the semiconductor-surface-electrodes are made; (2) vias are made in via holes in the insulating layer which electrically and directly connect the semiconductor-surface-electrodes and the mount-surface-electrodes; (3) via holes are filled with solder or electric conductive paste; and (4) an insulating layer which holds the semiconductor layers. Furthermore, Applicants note the Examiner did not assert that LOWERY teaches or suggests the above-noted features of the present invention, and only relied upon LOWERY for its purported teachings of the features of claim 4. Thus, Applicants submit no reasonable combination of these documents renders unpatentable the presently claimed invention.

Accordingly, for at least these reasons, Applicants request the Examiner withdraw the rejection of claim 4, and indicate claim 4 as allowable.

CONCLUSION

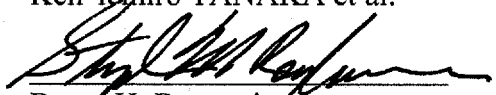
In view of the foregoing, the Examiner is respectfully requested to reconsider and withdraw the rejections of record, and allow each of the pending claims.

Applicants therefore respectfully request that an early indication of allowance of the application be indicated by the mailing of the Notices of Allowance and Allowability.

Authorization is hereby given to charge any fees necessary for the consideration of this amendment to deposit account No. 19-0089.

Should the Examiner have any questions regarding this application, the Examiner is invited to contact the undersigned at the below-listed telephone number.

Respectfully submitted,
Ken' ichiro TANAKA et al.



Bruce H. Bernstein
Reg. No. 29,027

GREENBLUM & BERNSTEIN, P.L.C.
1950 Roland Clarke Place
Reston, VA 20191
(703) 716-1191